IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A core cell, the core cell fabricated on a substrate, comprising; ~~upon~~

~~a~~ the substrate being defined of three columns of substrate material, the three columns of substrate material comprising a first p-type ~~n-type~~ column, a first n-type ~~p-type~~ column and a second p-type ~~n-type~~ column, the n-type ~~p-type~~ column being positioned between the first and second p-type columns; and

a pair of bitlines coupled to the core cell, such that the bitlines are separated by at least one of a voltage supply line and a ground voltage line, the bitlines not running in parallel immediately adjacent to one another.

2. (Original) The core cell of claim 1, wherein the bitline and complementary bitline are separated by one of at least a ground line and a voltage supply line.

3. (Cancelled)

4. (Currently amended) In a random access memory comprised of at least a plurality of core cells, a core cell, comprising:

first p-type ~~n-type~~ substrate;

first n-type ~~p-type~~ substrate; ~~and~~

second p-type ~~n-type~~ substrate, the first and second p-type ~~n-type~~ substrates being positioned on opposite sides of the first n-type ~~p-type~~ substrate; and

a pair of bitlines coupled to the core cell, wherein the bitlines are separated by at least one of a voltage supply line and a ground voltage line, the bitlines not running in parallel immediately adjacent to one another.

5. (Original) The core cell of claim 4, wherein each substrate has a generally rectangular shape, the rectangles having substantially the same area.

6. (Currently amended) The core cell of claim 4, wherein at least two PMOS transistors are fabricated on the first n-type ~~p-type~~ substrate.

7. (Currently amended) The core cell of claim 6, wherein at least 4 NMOS transistors are fabricated on the first and second p-type ~~n-type~~ substrate.

8. (Original) The core cell of claim 7, wherein the two PMOS transistors and two NMOS transistors are coupled together to form two inverters, the two inverters being coupled together to form the core cell's storage element.

9. (Cancelled)

10. (Cancelled).